REMARKS

In the patent application, claims 14-22 are pending. In the Final Office Action, all pending claims are rejected. In rejecting the claims, the Examiner cites *Lanzerotti et al.(*Si/SiGeC/Si Heterojunction BipolarTransistor, IEEE Electron Device Letters, Vol. 17, pp.334-337), and *Lanzerotti et al.* (Suppression of Boron Outdiffusion in SiGe HBTs by Carbon Incorporation, IEDM 96, pp.249-252), in view of *Sato et al.*(U.S. Patent No. 5,323,032). The Examiner alleges that cited *Lanzerotti* and *Sato* et al. references disclose a heterojunction bipolar transistor as claimed. Applicant has canceled claims 14-22 without prejudice.

The antecedent support for new claims 23- 43 can be found in the specification and the drawings.

The support for claims 23 and 24 can be found on p.3, lines 5-9, and lines 16-18.

The support for claim 25 can be found on p.3, lines 5-9, and p.6, first paragraph.

The support for claims 30 and 31 can be found on p.4, lines 16-17.

The support for claims 32 and 33 can be found on p.4, lines 14-16.

The support for claim 34 and 36 can be found on p.4, lines10-14.

The support for claim 37 can be found on p.6, line 31- p.7, line1; and in Figure 4.

The support for claim 38 can be found on p.7, second paragraph, and in Figure 5.

The support for claim 39 can be found on p.7, third paragraph, and in Figure 6.

The support for claims 40 and 41 can be found on p.3, lines 20-24.

The support for claim 42 can be found in Figure 3: implantation region (36).

The support for claim 43 can be found on p.6, lines 7-9.

On new matter has been introduced by way of amendment.

In claims 23, 24 and 43, the limitation that the change in the lattice by the incorporation of carbon is less than 5 parts per thousand. The change is that of the lattice constant. This change can only be inferred by incorporation on lattice sites that introduces a tensile strain component, which acts to compensate the compressive strain induce by Ge in a SiGe layer.

Since the strain in a lattice causes the creation of lattice defects that relief the strain. Such defects can lead to an undesirable operation of a transistor, especially at high frequency operations. None of the cited references teaches the limitation. Thus, claims 23, 24 and 43 are distinguishable over the cited *Lanzerotti* and *Sato* references.

Claim 25 includes the limitation that the base layer is disposed between the emitter layer and the collector layer such that one side of the base layer is immediately adjacent to the emitter and the other side of the base layer is immediately adjacent to the collector layer. It is respectfully submitted that, in the device as disclosed in *Lanzerotti* (IEEE), a spacer layer is disposed on each side of the base layer (p. 334, col.2, second paragraph describing Figure 1). Similarly, in the device as disclosed in *Lanzerotti* (IEDM), a spacer layer is disposed on each side of the base layer (p.249, col.2, first paragraph). This means that, in the device as disclosed in *Lanzerotti* (IEEE. IEDM), the base layer is not disposed immediately adjacent to the emitter layer and to the collector layer). Thus, claim 25 is distinguishable over the cited *Lanzerotti* and *Sato* references.

As for claims 26-42, they are dependent from claim 25 and recite features not recited in Claim 25. For reasons regarding claim 25 above, it is respectfully submitted that claims 26-42 are distinguishable over the cited *Lanzerotti* and *Sato* references.

CONCLUSION

Applicant has canceled claims 14-22 without prejudice. Applicant has added new claims 23-43, which are distinguishable over the cited *Lanzerotti* and *Sato* references. Early allowance of claims 23-43 is earnestly solicited.

Respectfully submitted,

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